REMARKS

The Examiner has stated that claims 12-24 are allowed. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter.

In view of the Examiner's earlier restriction requirement, Applicants retain the right to present claims 25-28 in a divisional application.

The Examiner rejected claims 1 and 11 under 35 U.S.C. §102(e) as being unpatentable over Shinogi et al. (US/6,534,387).

The Examiner rejected claims 2 and 4-9 under 35 U.S.C. 103(a) as being unpatentable over Shinogi et al. in view of Bhattacharya et al. (US/4,434,434).

The Examiner rejected claim 10 under 35 U.S.C. 103(a) as being unpatentable over Shinogi et al. in view of Miyamoto et al. (US/6,342,434).

The Examiner rejected claim 3 under 35 U.S.C. 103(a) as being unpatentable over Shinogi et al. over Bhattacharya et al. (US/4,434,434) as applied to claim 2 and in further view of Desai et al. (US/5,159,535).

Applicants respectfully traverse the §102(e) rejection with the following arguments.

35 USC § 102

As to claim 1, the Examiner states that "Shinogi et al. disclose a method of forming a semiconductor interconnect comprising a first step of providing a semiconductor wafer (20) (see Fig. 8A); as second step of forming bonding pads (8) (see Fig. 8B) in a terminal wiring level on the front side of the wafer (20); a third step of reducing the thickness of the wafer (see Figs. 8C and 9A); a fourth step of forming solder bumps (12) (see Fig. 9B) on the bonding pads (8); and a fifth step of dicing the wafer into bumped semiconductor chips (see Fig. 9C)."

Applicants contend that claim 1, as amended, is not anticipated by Shinogi et al. because Shinogi et al. does not teach each and every feature of claim 1. In a first example, Shinogi et al. does not teach "reducing the thickness of said wafer *prior* to any dicing operation on said semiconductor wafer." Applicants respectfully point out that Shinogi et al. specifically teaches in col. 2, lines 56-57 and in FIG. 8A that "As seen from FIG. 8A, after metal posts (8) are formed on wafer (20), grooves (21) are formed by a first dicing step." Clearly, a dicing operation has been performed *prior* to "reducing the thickness of said wafer" in violation of Applicants claim. In a second example, Shinogi et al. does not teach "dicing said wafer into *individual* bumped semiconductor chips." Applicants respectfully point out that Shinogi et al. specifically teaches in col. 2, lines 59-63 and in FIG. 8C that "Further, as seen from FIG. 8C, the wafer is divided into *individual* chips (20A) *by polishing* the rear surface of the wafer to reach the bottom of each of the grooves (21) (In this case, the *individual* chips(20a) are integrated by the resin R." Clearly, *individual* chips have been formed by polishing and not by *dicing* as Applicants claim requires. Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Shinogi et al. and is in condition for allowance. Since

claims 1-11 and 29-30 depend from claim 1, Applicants respectfully maintain that claims 1-11 and 29-30 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR: Gardecki et al.

Dated: 01/07/2005

BY:
Jack P. Friedman
Reg. No. 44,688
FOR:
Anthony M. Palagonia
Registration No.: 41,237

3 Lear Jet Lane, Suite 201
Schmeiser, Olsen & Watts
Latham, New York 12110
(518) 220-1850
Agent Direct Dial Number: (802)-899-5460